UTILITY PATENT APPLICATION AND FEE TRANSMITTAL

Attorney Docket No. 15.14/5048

ASSISTANT COMMISSIONER FOR PATENTS
Box PATENT APPLICATION
Washington, D.C. 20231

Express Mail Label No.: EL 484 106 738 US
Inventor(s): Tomoyuki FURUHATA and Atsushi YAMAZAKI
For: SEMICONDUCTOR DEVICES
HAVING A NON-VOLATILE MEMORY TRANSISTOR

APPLICATION ELEMENTS:

X 25 pages of Specification including an Abstract of the disclosure
X 15 Sheets of drawings (□ informal ■ formal)
__ Declaration and Power of Attorney.
__ An assignment of the invention to _____ with Recordation Cover Sheet.
__ Certified Copy(ies) of claimed priority document(s) no. 11-177146 filed June 23, 1999 X WILL FOLLOW
__ IDS enclosed. __ with references.
X Return Receipt Postcard.

CALCULATION OF FEES

	ITEM	NO. OF CLAIMS FILED MINUS BASE*	NO. OF CLAIMS OVER BASE	X SM/LG ENTITY FEE	$ AMOUNT	$ FEE
A	TOTAL CLAIMS FEE	23 - 20* =	3	X $9 or X $18	$54	
B	INDEPENDENT CLAIMS FEE**	2 - 3* =	0	X $39 or X $78	$	
C	SUBTOTAL - ADDITIONAL CLAIMS FEE (ADD FINAL COLUMN IN LINES A + B)					$54
D	MULTIPLE-DEPENDENT CLAIMS FEE			SMALL ENTITY FEE = $130 LARGE ENTITY FEE = $260		$
E	BASIC FEE*			SMALL ENTITY FEE = $345 LARGE ENTITY FEE = $690		$690
F	TOTAL FILING FEE (ADD TOTALS FOR LINES C, D, AND E)					$744
G	ASSIGNMENT RECORDING FEE				$ 40	$
H	INTERNATIONAL TYPE SEARCH REPORT				$40	$
	**LIST INDEPENDENT CLAIMS 1 and 19					

_ Please charge my Deposit Account No. 50-0585 the amount of $0 **A copy of this letter is enclosed.**

X A check in the amount of $744 to cover the filing fee is enclosed.

_ A check in the amount of $0 to cover Assignment Recordation fee is enclosed.

X The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. 50-0585. **A copy of this sheet is enclosed.**
X Any additional filing fees required under 37 CFR 1.16.
X Any patent application processing fees under 37 CFR 1.17.
__ The Commissioner is hereby authorized to charge payment of the following fees during the pendency of this application or credit any overpayment to Deposit Account No. 01-1651.
__ Any patent application processing fees under 37 CFR 1.17.
__ The issue fee set in 37 CFR 1.18 at or before mailing of the Notice of Allowance, pursuant to 37 CFR 1.311(b).
__ Any filing fees under 37 CFR 1.16 for presentation of extra claims.

Respectfully submitted,

Date: June 23, 2000

Alan S. Raynes
Reg. No. 39,809

KONRAD RAYNES & VICTOR LLP
1180 South Beverly Drive, Suite 501
Los Angeles, California 90035
310-556-7983

F:\CLIENTS\SeikoEpson\0015.0014\APPLN.TRX.KRV.frm

6-26-00

A

EL 484 106 738 US
PATENT
15.14/5048

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:
FURUHATA, et al.

Serial No: NEW
Filed: June 23, 2000

Art Unit: unassigned
Examiner: unassigned

For: SEMICONDUCTOR DEVICES
HAVING A NON-VOLATILE MEMORY TRANSISTOR

CERTIFICATE OF MAILING VIA U.S. EXPRESS MAIL
"Express Mail" Mailing Label No. EL 484 106 738 US
Date of Deposit: June 23, 2000

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

I hereby certify that

X	two copies of a letter of transmittal
X	check in amount of $ 744 as filing fee
X	patent application (24 pages of specification; 23 claims; 1 page of abstract) under 37 CFR 1.53 (b)
X	return postcard

are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service with sufficient postage under 37 CFR 1.10 on the date indicated above and are addressed to:

Box Patent Application
Assistant Commissioner for Patents
Washington, D.C. 20231.

June 23 2000
Date of Deposit

Alan S. Raynes
Name of person mailing papers

Alan S. Raynes
Signature

F:\CLIENTS\SeikoEpson\0015.0014\CERT.EXP.wpd

SEMICONDUCTOR DEVICES HAVING A NON-VOLATILE MEMORY TRANSISTOR

Inventors: Tomoyuki Furuhata, Atsushi Yamazaki

The copending and commonly assigned patent application entitled "Methods for Manufacturing Semiconductor Devices Having a Non-Volatile Memory Transistor", with Tomoyuki Furuhata and Atsushi Yamazaki listed as inventors, with docket no. 15.15/5049, is hereby incorporated by reference in its entirety. The copending and commonly assigned patent application entitled "Non-Volatile Semiconductor Memory Devices", with Tomoyuki Furuhata and Atsushi Yamazaki listed as inventors, with docket no. 15.16/5050, is hereby incorporated by reference in its entirety. Japanese patent application no. 11-177146, filed June 23, 1999, is hereby incorporated by reference in its entirety.

Technical Field

The present invention relates to semiconductor devices having a non-volatile memory transistor with a split-gate structure and includes a semiconductor device comprising a plurality of field effect transistors having different operation voltages.

Background

In recent years, a mixed-mounting of various circuits has been utilized in view of various demands such as a shortened chip-interface delay, a lowered cost per circuit board, a lowered cost in design and development of a circuit board and the like. A mixed-mounting technology for mounting memory and logic has become one of the important technologies. However, such a mixed-mounting technology presents problems that result in complex processes and higher costs for manufacturing ICs.

Summary

Certain embodiments relate to a semiconductor device comprising a memory region including a split-gate non-volatile memory transistor. The device also includes a first transistor region including a first voltage-type transistor that operates at a first voltage level, a second transistor region including a second voltage-type transistor that operates at a second voltage level, and a third transistor region including a third voltage-type transistor that operates at a third voltage level. The second voltage-type transistor includes a gate insulation layer formed from at least two insulation layers.

In one aspect of certain embodiments, the second voltage-type transistor described above includes a gate insulation layer that is formed in the same step in which a gate insulation layer of the first voltage-type transistor is formed.

In another aspect of certain embodiments, the third voltage-type transistor described above includes a gate insulation layer formed from at least three insulation layers. Additionally, the third voltage-type transistor may include an insulation layer that is formed in the same step in which the gate insulation layer of the first voltage-type transistor is formed.

In yet another aspect of certain embodiments, the non-volatile memory transistor described above may include a source, a drain, a gate insulation layer, a floating gate, an intermediate insulation layer adapted to function as a tunnel insulation layer, and a control gate. The intermediate insulation layer may be formed from at least three insulation layers, with the first and second outermost layers of the three insulation layers, respectively, contacting the floating gate and the control gate. The first and second outermost layers may also be composed of insulation layers that are formed by a thermal oxidation method.

Still other embodiments related to an embedded semiconductor device, the embedded semiconductor device a plurality of semiconductor devices selected from the group consisting of a flash-memory, an SRAM memory, a RISC, an analog circuit, and an interface circuit. The plurality of semiconductor devices are embedded in an SOG. At least one of the semiconductor devices comprises a structure including a memory region including a split-gate non-volatile memory transistor and three transistor regions. The first

transistor region includes a first voltage-type transistor that operates at a first voltage level. The second transistor region includes a second voltage-type transistor that operates at a second voltage level that is greater than the first voltage level. The third transistor region includes a third voltage-type transistor that operates at a third voltage level that is greater than the second voltage level. The second voltage-type transistor includes a gate insulation layer formed from at least two insulation layers.

Brief Description of the Drawings

Certain embodiments of the invention are described with reference to the accompanying drawings which, for illustrative purposes, are schematic and not necessarily drawn to scale.

Fig. 1 is a schematic cross-sectional view of a semiconductor device in accordance with an embodiment of the present invention.

Figs. 2 - 13 illustrate cross-sectional views of a wafer during manufacturing for forming the semiconductor device shown in Fig. 1 according to embodiments of the present invention.

Fig. 14 is a schematic plan view of an embedded semiconductor device employing a semiconductor device in accordance with one embodiment of the present invention.

Fig. 15 shows a block diagram of a flash-memory of the embedded semiconductor device shown in Fig. 14.

Detailed Description

Certain embodiments of the present invention relate to methods for manufacturing a semiconductor device having highly reliable non-volatile memory transistors including field effect transistors that are operated at a plurality of different voltage levels, in which gate insulation layers of the transistors are formed by fewer and common manufacturing steps.

One embodiment of the present invention provides a semiconductor device having a non-volatile memory transistor, the semiconductor device comprising a memory region, first, second and third transistor regions including field effect transistors that operate at different voltage levels. The memory region includes a split-gate non-volatile memory

transistor. The first transistor region includes a first voltage-type transistor that operates at a first voltage level. The second transistor region includes a second voltage-type transistor that operates at a second voltage level. The third transistor region includes a third voltage-type transistor that operates at a third voltage level. The second voltage-type transistor has a gate insulation layer formed from at least two insulation layers, and includes an insulation layer that is formed in the same step in which a gate insulation layer of the first voltage-type transistor is formed.

In one aspect of certain embodiments, the first through the third voltage-type transistors operate at at least three different voltage levels, i.e., the first through the third voltage levels. Therefore, logic operable at these voltage levels can be mounted in the semiconductor device. Because of the voltage-type transistors, logic that may be required for the operation of the non-volatile memory transistors as well as other circuit regions can be mixed and mounted.

Also, the gate insulation layer of the second voltage-type transistor may be formed from at least two insulation layers, and one of the insulation layers may be formed in the same step in which the gate insulation layer of the first voltage-type transistor is formed. As a result, the number of manufacturing steps is reduced.

In addition, the third voltage-type transistor has a gate insulation layer preferably formed from at least three insulation layers, and may preferably include an insulation layer that is formed in the same step in which the gate insulation layer of the first voltage-type transistor is formed. As a result, each of the gate insulation layers of the second and the third voltage-type transistors includes an insulation layer that is formed in the same step in which the gate insulation layer of the first voltage-type transistor is formed. This further reduces the number of manufacturing steps.

The split-gate type non-volatile memory transistor may include a source, a drain, a gate insulation layer, a floating gate, an intermediate insulation layer that functions as a tunnel insulation layer and a control gate. The intermediate insulation layer may preferably be composed of at least three layers, and preferably includes first and second outermost layers that respectively contact the floating gate and the control gate, wherein the outermost layers are composed of silicon oxide layers that are formed by a thermal oxidation method.

Because the outermost layers contact the floating gate and the control gate, the respective interface states stabilize. As a result, the electric charge transfer by FN conduction (Fowler-Nordheim tunneling) is stably conducted, and thus the operation of the non-volatile memory transistor stabilizes. Further, the outermost layer that contacts the control gate of the intermediate insulation layer may preferably be formed in the same step in which the gate insulation layer of the first voltage-type transistor is formed. As a result, the number of manufacturing steps is further reduced.

The gate insulation layer of the third voltage-type transistor may preferably be formed in the same step in which the intermediate insulation layer of the non-volatile memory transistor is formed. As a result, the number of manufacturing steps is further reduced.

The film thickness of the gate insulation layer of each of the voltage-type transistors may preferably be in the following ranges, in consideration of the dielectric strength of the voltage-type transistors. The gate insulation layer of the first voltage-type transistor may preferably have a film thickness of 3 – 13 nm. The gate insulation layer of the second voltage-type transistor may preferably have a film thickness of 4 – 15 nm. The gate insulation layer of the third voltage-type transistor may preferably have a film thickness of 16 – 45 nm.

The intermediate insulation layer of the non-volatile memory transistor may preferably have a film thickness of 16 – 45 nm, in consideration of the characteristics of the tunnel insulation layer. Further, the first outermost layer that forms the intermediate insulation layer of the non-volatile memory transistor may preferably have a film thickness of 5 – 15 nm, and the second outermost layer may preferably have a film thickness of 1 – 10 nm.

Each of the voltage-type transistors described above may, for example, preferably be operated at a voltage level in the following ranges: The first voltage level that operates the first voltage-type transistor is at 1.8 – 3.3 V in an absolute value, the second voltage level that operates the second voltage-type transistor is at 2.5 – 5 V in an absolute value, and the third voltage level that operates the third voltage-type transistor is at 10 – 15 V in an absolute value.

A semiconductor device obtained by the manufacturing method of certain embodiments of the present invention may further comprise a flash-memory (flash EEPROM), and include a memory cell array of non-volatile memory transistors and a peripheral circuit formed therein. Also, the semiconductor device may further be mixed with other circuit regions such as logic regions mounted therein. The circuit regions may include, for example, cell-base circuits, memory circuits such as ROMs and RAMs, RISC (reduced instruction set computer), IP (intellectual property) macros, and analog circuits.

The first voltage-type transistor may, for example, be included in at least one circuit selected from a group consisting of a Y-gate, sense amplifier, an input/output buffer, an X-address decoder, a Y-address decoder, an address buffer and a control circuit.

The second voltage-type transistor may, for example, be included in at least one circuit selected from a group consisting of a Y-gate, sense amplifier, an input/output buffer, an X-address decoder, a Y-address decoder and an interface circuit.

The third voltage-type transistor may, for example, be included in at least one circuit selected from a group consisting of a voltage generation circuit, an erase voltage generation circuit and a step-up voltage circuit.

Fig. 1 schematically shows a cross-sectional view of a semiconductor device including a non-volatile memory transistor in accordance with an embodiment of the present invention. The semiconductor device includes a memory region 4000, a first transistor region 1000, a second transistor region 2000 and a third transistor region 3000.

The memory region 4000 includes a non-volatile memory transistor with a split-gate structure (hereinafter referred to as "memory transistor") 400. The first transistor region 1000 includes a first voltage-type transistor 100 that operates at a first voltage level V1 (preferably 1.8 – 3.3 V in an absolute value). The second transistor region 2000 includes a second voltage-type transistor 200 that operates at a second voltage level V2 (preferably 2.5 – 5 V in an absolute value). The third transistor region 3000 includes a third voltage-type transistor 300 that operates at a third voltage level V3 (preferably 10 – 15V in an absolute value). Embodiments of circuits that use the first through the third voltage-type transistors 100, 200 and 300 will be described below.

The memory transistor 400, the first voltage-type transistor 100, the second voltage-type transistor 200 and the third voltage-type transistor 300 are respectively formed in wells 12 that are formed in a P-type silicon substrate 10. The memory region 4000 and the first through the third transistor regions 1000, 2000 and 3000 are respectively isolated from one another by field insulation layers 18. Also, the transistors in the respective regions 1000 through 4000 are isolated by field insulation layers (not shown) formed in predetermined patterns. In the embodiment shown in the figure, each of the transistors is formed in each of the wells. However, when wells are not required, they may be formed in the substrate. For example, N-channel type memory transistors or N-channel type second voltage-type transistors may be formed in the substrate, but not in wells.

The first through the third transistor regions 1000, 2000 and 3000 and the memory region 4000 may respectively include N-channel type and P-channel type transistors. However, for the simplicity of description, Fig. 1 shows transistors of either one of the conductivity types.

The memory transistor 400 has a source 16 and a drain 14 composed of N^+ type impurity diffusion layers formed in a P-type well 12, and a gate insulation layer 26 formed on the surface of the well 12. A floating gate 40, an intermediate insulation layer 50 and a control gate 36 are formed on the gate insulation layer 26.

Further, a selective oxide insulation layer 42 is formed on the floating gate 40. The selective oxide insulation layer 42 is formed by selective oxidation on a part of a polycrystal silicon layer that becomes the floating gate, as described below, and has a preferred structure in which the thickness thereof becomes thinner from its center toward its end sections. As a result, upper edge sections of the floating gate 40 form sharp edges, such that an electric field concentration is apt to occur at the upper edges of the floating gate 40.

The thickness of the gate insulation layer 26 of the memory transistor 400 may preferably be 6 – 9 nm, in consideration of the dielectric strength of the memory transistor 400.

The intermediate insulation layer 50 continues from the top surface of the selective oxide insulation film 42 to the side surface of the floating gate 40, further extends along the surface of the silicon substrate 10 and reaches one end of the source 16. The intermediate

insulation layer 50 functions as what is referred to as a tunnel insulation layer. Further, the intermediate insulation layer 50 is composed of three insulation layers (silicon oxide layers), which are, in the order from the bottom, a first insulation layer 50a, a second insulation layer 50b and a third insulation layer 50c. The first and the third insulation layers 50a and 50c are composed of silicon oxide layers that are formed by a thermal oxidation method. The second insulation layer 50b is composed of a silicon oxide layer that is formed by a CVD method.

The intermediate insulation layer 50 may preferably have a film thickness of 16 – 45 nm, in consideration of its function as a tunnel insulation layer. The first insulation layer 50a may preferably have a film thickness of 5 – 15 nm, the second intermediate insulation layer 50b may preferably have a film thickness of 10 – 20 nm, and the third insulation layer 50c may preferably have a film thickness of 1 – 10 nm.

The intermediate insulation layer 50 that functions as a tunnel insulation layer has a three-layer structure, and the first insulation layer (a first outermost layer) 50a and the third insulation layer (a second outermost layer) 50c that respectively contact the floating gate 40 and the control gate 36 are preferably formed from thermal oxidation films. As a result, the interface state between the floating gate 40 and the first insulation layer 50a stabilizes, and the interface state between the control gate 36 and the third insulation layer 50c stabilizes. As a consequence, the transfer of the charge by the FN conduction from the floating gate 40 through the intermediate insulation layer 50 to the control gate 36 becomes stable, and thus the operation of the memory transistor 400 stabilizes. This contributes to an increase in the number of data writing/erasing operations (cycle life) of the memory transistor 400.

Also, because the intermediate insulation layer 50 has the second insulation layer 50b that is composed of a silicon oxide layer which is formed by a CVD method, the dielectric strength between the floating gate 40 and the control gate 36 increases. Also, malfunctions that may occur at the time of writing in or reading from memory cells, namely, write disturbs and read disturbs, can be inhibited.

The first voltage-type transistor 100, when it is a P-channel type MOS transistor, for example, has a source 16 and a drain 14 that are composed of P^+ type impurity diffusion layers which are formed in the N-type well 12, a first gate insulation layer 20 and a first gate

electrode 30. The first voltage-type transistor 100 is preferably driven at a first voltage level V1 (1.8 – 3.3 V in an absolute value). The first gate insulation layer 20 may preferably have a film thickness of 3 – 13 nm, in consideration of the dielectric strength of the first voltage-type transistor 100.

The second voltage-type transistor 200, when it is an N-channel type MOS transistor, for example, has a source 16 and a drain 14 that are composed of N^+ type impurity diffusion layers which are formed in the P-type well 12, a second gate insulation layer 22 and a second gate electrode 32. The second gate insulation layer 22 is composed of two silicon oxide layers, namely, a first insulation layer 22a and a second insulation layer 22b. The second insulation layer 22b is formed in the same step in which the first gate insulation layer 20 of the above-described first voltage-type transistor 100 is formed.

The second voltage-type transistor 200 is preferably driven at a second voltage level (2.5 – 5 V in an absolute value). The second gate insulation layer 22 may preferably have a film thickness of 4 – 15 nm, in consideration of the dielectric strength of the second voltage-type transistor 200. Also, the thickness of the first insulation layer 22a may preferably be 3 – 15 nm, and the thickness of the second insulation layer 22b may preferably be 1 – 10 nm.

The third voltage-type transistor 300, when it is a P-channel type MOS transistor, for example, has a source 16 and a drain 14 that are composed of P^+ type impurity diffusion layers which are formed in the N-type well 12, a third gate insulation layer 24 and a third gate electrode 34. The third gate insulation layer 24 is formed from three silicon oxide layers, which are, in the order from the bottom, a first insulation layer 24a, a second insulation layer 24b and a third insulation layer 24c. The insulation layers 24a, 24b and 24c may preferably be formed in the same steps in which the first insulation layer 50a, the second insulation layer 50b and the third insulation layer 50c that form the intermediate insulation layer 50 of the memory transistor 400 are formed, respectively.

The third voltage-type transistor 300 is preferably driven at a third voltage level V3 (10 – 15 V in an absolute value). The third gate insulation layer 24 may preferably have a film thickness of 16 – 45 nm, in consideration of the dielectric strength of the third voltage-type transistor 300. The first insulation layer 24a may preferably have a film thickness of 5

– 15 nm, the second insulation layer 24b may preferably have a film thickness of 10 – 20 nm, and the third insulation layer 24c may preferably have a film thickness of 1 – 10 nm.

An interlayer dielectric layer 600 is formed on the wafer in which the memory transistor 400 and the first through the third voltage-type transistors 100, 200 and 300 are formed. The interlayer dielectric layer 600 defines contact holes that reach the sources 16, the drains 14 and the gate electrode of each of the transistors 100, 200, 300 and 400. Contact conductive layers are formed in the contact holes. A wiring layer 80 having a predetermined pattern is formed on the interlayer dielectric layer 600. It is noted that Fig. 1 partially shows the contact conductive layers and wiring layers.

The semiconductor device of this embodiment has the first through the third transistor regions 1000, 2000 and 3000 in which the first through third voltage-type transistors 100, 200 and 300 that respectively operate at at least three different voltage levels (V1, V2 and V3) are formed. According to this semiconductor device, the memory transistor 400 in the memory region 4000 is operable. In the semiconductor device, not only logic for operating a flash EEPROM can be implemented, but also a flash EEPROM and other circuits that are operated at different voltage levels may be mixed and implemented in the same substrate to construct a system LSI. Such circuits include interface circuits, gate array circuits, memory circuits such as RAMs and ROMs and RISCs (reduced instruction set computer), or a variety of IP (Intellectual Property) macro circuits, or other digital circuits and analog circuits.

Methods for operating a memory transistor, an embedded semiconductor device in which a semiconductor device according to an embodiment of the present invention is applied, and methods for manufacturing a semiconductor device shown in Fig. 1 will be described below.

For the operation of a memory transistor with a split-gate structure 400 in accordance with certain embodiments of the present invention, a channel current flows between the source 16 and the drain 14 to thereby inject a charge (hot electrons) in the floating gate 40 when data is written. When data is erased, a predetermined high voltage is applied to the control gate 36 to thereby transfer the charge stored in the floating gate 42 to the control gate 36 by the FN conduction. Each of the operations will be described below.

First, an example of a writing operation will be described. For the data-writing operation, the source 16 is set at a higher potential with respect to the drain 14, and a low potential is applied to the control gate 36. As a result, hot electrons that are generated under the floating gate 40 and near the drain 14 are accelerated towards the floating gate 40, and injected in the floating gate 40 through the gate insulation layer 26 to thereby accomplish the data-writing operation.

In the writing operation, for example, the control gate 36 is set at a potential (Vc) of 2 V, the source 16 is set at a potential (Vs) of 9 V, and the drain 14 is set at a potential (Vd) of 0 V. The well 12 is set at a potential (Vwell) of 0 V.

Next, an example of an erasing operation will be described. For the erasing operation, the control gate 36 is set at a potential higher than the potential of the source 16 and the drain 14. As a result, the charge stored in the floating gate 40 is discharged through the sharp upper edge section of the floating gate 40 by the FN tunneling conduction, passing through the intermediate insulation layer 50, to the control gate 36, whereby the data is erased.

In the erasing operation, for example, the control gate 36 is set at a potential (Vc) of 12 V, the source 16 and the drain 14 are set at potentials (Vs) and (Vd) of 0 V. The well 12 is set at a potential (Vwell) of 0 V.

Next, an example of a reading operation will be described. For the reading operation, the drain 14 is set at a higher potential than the source 16, and the control gate 36 is applied with a predetermined potential, whereby a determination is made based on the presence or the absence of a formed channel as to whether or not data is written. More specifically, when a charge is injected in the floating gate 40, the potential of the floating gate 40 becomes low, with the result that a channel is not formed and a drain current does not flow. On the other hand, when the floating gate 40 is not injected with a charge, the floating gate 40 has a high potential, with the result that a channel is formed and a drain current flows. By detecting a current flowing from the drain 14 by a sense amplifier, data in the memory transistor 400 can be read out.

In the reading operation, for example, the control gate 36 is set at a potential (Vc) of 3 V, the source 16 is set at a potential (Vs) of 0 V, and the drain 14 is set at a potential (Vd) of 2 V. The well 12 is set at a potential (Vwell) of 0 V.

The operations described above are examples, and other operation conditions are also applicable in accordance with other embodiments. For example, table 1 below sets forth a range of voltages according to one embodiment for write, erase and read operations.

Table 1. Range of voltages for write, erase and read operations according to one embodiment.

	control gate (V)	source (V)	drain (V)
write	0.5 - 3	8 - 11	0
erase	10 - 14	0	0
read	1 - 5	0	1 - 5

Fig. 14 schematically shows a layout of an embedded semiconductor device 5000 in which a semiconductor device of an embodiment of the present invention is implemented. In accordance with this embodiment, the embedded semiconductor device 5000 includes a flash-memory (flash EEPROM) 90, an SRAM memory 92, a RISC 94, an analog circuit 96 and an interface circuit 98 that are mixed and mounted in an SOG (sea of gates) structure.

Fig. 15 shows a block diagram of a structure of a flash-memory. The flash-memory includes a memory cell array 1 in which memory transistors are disposed in an array, a Y-gate, sense amplifier 2, an input/output buffer 3, an X-address decoder 4, a Y-address decoder 5, an address buffer 6 and a control circuit 7.

The memory cell array 1 corresponds to the memory region 4000 shown in Fig. 1 and has a plurality of split-type memory transistors 400 disposed in a matrix. The memory cell array 1 connects to the X-address decoder 4 and the Y-gate 2 in order to select rows and columns of the memory cell array 1. The Y-gate 2 connects to the Y-address decoder 5 that provides column selection data. The X-address decoder 4 and the Y-address decoder 5 connect to the address buffer 6 that temporarily stores address data.

The Y-gate 2 connects to a write-voltage generation circuit (not shown) for conducting a data-wiring operation, and to a sense amplifier for conducting a data-reading operation. The X-address decoder connects to an erasing-voltage generation circuit for conducting a data-erasing operation. The write-voltage generation circuit and the sense amplifier 2 connect to the input/output buffer 3 that temporarily stores input and output data. The address buffer 6 and the input/output buffer 3 connect to the control circuit 7 that controls the operation of the flash-memories. The control circuit 7 performs the control operation based on chip enable signals, output enable signals and program signals.

In the embedded semiconductor device 5000, transistors operable at different voltage levels are selected depending on the operation voltages of the respective circuits.

The first voltage-type transistor 100 that is operated at a first voltage level is included in, for example, at least one of the Y-gate, sense amplifier, the input/output buffer, the X-address decoder, the Y-address decoder, the address buffer, the control circuit, the SOG and the gate array.

The second voltage-type transistor 200 that is operated at a second voltage is included in, for example, at least one of the Y-gate, sense amplifier, the input/output buffer, the X-address decoder, the Y-address decoder and the interface circuit.

The third voltage-type transistor 300 that is operated at a third voltage is included in, for example, at least one of the writing-voltage generation circuit, the erasing-voltage generation circuit and the step-up circuit.

Fig. 14 shows an example of a layout of the embedded semiconductor device 5000. The present invention is applicable to various types of system LSIs.

Next, a method for manufacturing a semiconductor device such as that shown in Fig. 1 in accordance with one embodiment of the present invention will be described with reference to Figs. 2 through 13.

(A) First, as shown in Fig. 2, a field insulation layer 18 is formed on the surface of a silicon substrate 10 in a predetermined region thereof by a selective oxidation method. Then, a P-type impurity (for example, boron) or an N-type impurity (for example, arsenic or phosphorous) is doped in the P-type silicon substrate 10 to thereby form a P-type well or an N-type well 12 in a predetermined region of the substrate 10.

Further, a silicon oxide layer 26L is formed on the surface of the silicon substrate 10 by, for example, a thermal oxidation method. The silicon oxide layer 26L becomes a gate insulation layer 26 of the memory transistor 400. The silicon oxide layer 26L may preferably have a thickness of 6 – 9 nm, in consideration of the gate dielectric strength.

(B) Then, as shown in Fig. 3, a polysilicon layer 40L is formed on the surface of the silicon oxide layer 26L by, for example, a CVD method. The polysilicon layer 40L becomes a floating gate 40 of the memory transistor 400. The polysilicon layer 40L may preferably have a thickness of 100 – 200 nm.

Then, a first silicon nitride layer 60L is formed on the surface of the polysilicon layer 40L. The first silicon nitride layer 60L may preferably have a thickness of 50 – 150 nm. Then, the silicon nitride layer 60L is selectively etched, using a resist layer R1 as a mask, to remove a predetermined region thereof. The region of the first silicon nitride layer 60L that is removed corresponds to a region where a selective oxide insulation layer 42 of the memory transistor 400 is formed.

Then, phosphorous or arsenic is diffused in the polysilicon layer 40L, using the resist layer R1 formed on the first silicon nitride layer 60L as a mask, to form an N-type polysilicon layer 40L. The polysilicon layer may be changed to N-type by other methods. For example, after the polysilicon layer is formed, the polysilicon layer is implanted with phosphorous ions or arsenic ions. Alternatively, after the polysilicon layer is formed, the polysilicon layer is contacted with a carrier gas containing phosphoryl chloride ($POCl_3$). Alternatively, when the polysilicon layer is formed, the layer is contacted with a carrier gas containing phosphine (PH_3).

Then, the resist layer R1 is removed.

(C) Next, as shown in Fig. 4, an exposed portion in the polysilicon layer 40L is selectively oxidized to form a selective oxide insulation layer 42 on the surface of the polysilicon layer 40L in a predetermined region thereof. The selective oxide insulation layer 42 formed by the selective oxidation preferably has a maximum film thickness at its central area, and gradually becomes thinner toward end sections thereof. The selective oxide insulation layer 42 may preferably have a film thickness of 100 – 200 nm at the thickest portion. Thereafter, the first silicon nitride layer 60L is removed.

(D) Next, as shown in Fig. 5, an etching is conducted, using the selective oxide insulation layer 42 as a mask, to selectively remove the polysilicon layer 40L.

By the steps described above, the gate insulation layer 26, the floating gate 40 and the selective oxide insulation layer 42 are formed in the memory region 4000.

(E) Then, as shown in Fig. 6, the silicon oxide layer 26L is removed by a wet-etching, and then a first silicon oxide layer 50aL (24aL) is formed on the surface of the wafer by a thermal oxidation method. The silicon oxide layer 50aL (24aL) becomes a first insulation layer 50a that forms an intermediate insulation layer 50 of the memory transistor 400, and a first insulation layer 24a that forms a gate insulation layer 24 of the third voltage-type transistor 300. The silicon oxide layer 50aL (24aL) may preferably have a thickness of 5 – 15 nm, for example.

The silicon oxide layer may preferably be formed by any one of the following thermal oxidation methods:

(a) a dry-oxidation is conducted at 700 – 1000°C;

(b) after the dry-oxidation conducted in step (a), a wet-oxidation is further conducted at 700 - 1000°C; and

(c) after step (a) or step (b), an anneal treatment is conducted in a nitrogen atmosphere at 700 - 1000°C for 10 – 30 minutes.

By conducting the dry-oxidation in step (a) described above, the size of polysilicon grains on the surface of the floating gate 40 becomes generally uniform, and the planarization of the surface of the floating gate 40 is improved. As a result, the interface state of the floating gate 40 becomes more stabilized, the electron capturing is reduced, and the cycle life of write/erase operations of the memory transistor is extended.

Further, when at least one of the wet-oxidation in step (b) and the anneal treatment in step (c) is added after the dry-oxidation in step (a), the silicon oxide layer 50aL is further densified, and the electron capturing is reduced, such that the film characteristics can be improved.

(F) Then, as shown in Fig. 7, a second silicon oxide layer 50bL (24bL) is further formed on the surface of the first silicon oxide layer 50aL (24aL). The second silicon oxide layer 50bL (24bL) is formed by a CVD method. The second silicon oxide layer 50bL

(24bL) becomes a second insulation layer 50b that forms an intermediate insulation layer 50 of the memory transistor 400, and a second insulation layer 24b that forms a gate insulation layer 24 of the third voltage-type transistor 300. The silicon insulation layer 50bL (24bL) has a thickness of 10 – 20 nm, for example.

Considering the density of the formed film, the permeability resistance against oxygen ions and the like in a thermal oxidation to be performed in a later stage, the CVD method used in this embodiment may preferably be conducted by a HTO (high temperature oxide) method, using monosilane or tetraethylorthosilicate, a TEOS (tetraethyl orthosilicate) method, using ozone as an oxidation agent or a plasma TEOS method. A preferred temperature range for an HTO method is about 700 - 900°C.

Next, a second silicon nitride layer 62L is formed on the surface of the silicon oxide layer 50bL (24bL). The second silicon nitride 62L may preferably have a film thickness of 10 – 20 nm. Due to the second silicon nitride layer 62L thus formed, although the second silicon nitride layer 62L will be removed in step (I) that is later performed, the intermediate insulation layer 50 of the memory transistor 400 and the gate insulation layer 24 of the third voltage-type transistor 300 do not unnecessarily become thick, and thus the film thickness can be precisely controlled. Then, an anneal treatment may be conducted at 700 – 1000°C for about 20 – 40 minutes to densify the insulation layers.

(G) Then, as shown in Fig. 8, a resist layer R3 defining an opening section in the second transistor region 2000 is formed. The second silicon nitride layer 62L, the upper silicon oxide layer 50bL and the lower silicon oxide layer 50aL in the transistor region 2000 may be removed by a dry-etching and a wet-etching, using the resist layer R3 as a mask. Then, the resist layer R3 is removed.

(H) Then, as shown in Fig. 9, the surface of the wafer is subjected to a thermal oxidation, for example, a wet-oxidation at 700 - 900°C, to thereby form a third silicon oxide layer 22aL on the surface of the wafer. The silicon oxide layer 22aL becomes a first insulation layer 22a that forms the gate insulation layer 22 of the second voltage-type transistor 200. The silicon oxide layer 22aL has a film thickness of 3 – 15 nm, for example.

(I) Then, as shown in Fig. 10, a resist layer R4 is formed on the surface of the silicon oxide layer 22aL in the second transistor region 2000. The second silicon nitride

layer 62L is removed by a dry-etching, using the resist layer R4 as a mask. Thereafter, the resist layer R4 is removed.

(J) Then, as shown in Fig. 11, a resist layer R5 defining an opening in the first transistor region 1000 is formed. The two silicon oxide layers 50bL and 50aL in the first transistor region 1000 are removed by a wet-etching, using the resist layer R5 as a mask. Then, the resist layer R5 is removed.

(K) Then, as shown in Fig. 12, the surface of the wafer is subjected to a thermal oxidation, for example, a wet-oxidation conducted at 700 - 900°C, to form a fourth silicon oxide layer 20L (50cL, 22bL, 24cL) on the surface of the wafer. The silicon oxide layer 20L becomes the gate insulation layer 20 of the first voltage-type transistor 100, the second insulation layer 22b that forms the gate insulation layer 22 of the second voltage-type transistor 200, the third insulation layer 24c that forms the gate insulation layer 24 of the third voltage-type transistor 300, and the third insulation layer 50c that forms the intermediate insulation layer 50 of the memory transistor 400. The silicon oxide layer 20L has a film thickness of 1 – 10 nm, for example.

The steps described above form the insulation layers that compose the intermediate insulation layer 50 of the memory transistor 400, the gate insulation layer 20 of the first voltage-type transistor 100, the gate insulation layer 22 of the second voltage-type transistor 200 and the gate insulation layer 24 of the third voltage-type transistor 300.

(L) Then, as shown in Fig. 13, a polysilicon layer is formed on the surface of the wafer in the same manner as conducted in step (C) described above. Alternatively, a polycide layer may be formed by a know method, instead of a polysilicon layer. A resist layer having a predetermined pattern is formed on the polysilicon layer, and then a patterning is conducted by an etching to form a gate insulation layer and a gate electrode of each of the memory transistor 400, the first voltage-type transistor 100, the second voltage-type transistor 200 and the third voltage-type transistor 300. In this embodiment, the etching is conducted in a manner that the silicon oxide layer remains to a preferred film thickness of 1 – 5 nm on exposed surfaces of the silicon substrate 10.

(M) Then, as shown in Fig. 1, an N-type impurity for an N-channel type transistor and a P-type impurity for a P-channel type transistor are doped in predetermined ones of the

wells 12 by a known method. As a result, impurity diffusion regions that compose the sources 16 and the drains 14 are formed.

Then, an interlayer dielectric layer 600 that is composed of a silicon oxide layer is formed by, for example, a CVD method on the surface of the wafer on which the transistors 100, 200 and 300 and the memory transistor 400 are formed. Then, the interlayer dielectric layer 600 is selectively etched to remove predetermined regions thereof to define contact holes that reach the sources 16 and the drains 14. Then, a conductive layer composed of an aluminum layer or the like is deposited on the interlayer dielectric layer 600 and in the contact holes by, for example, a sputtering method. The conductive layer is patterned to form metal wiring layers (for example, bit lines and source lines) 80 that electrically connect to the impurity diffusion regions.

In the manufacturing method described above, the memory transistor 400, the first voltage-type transistor 100, the second voltage-type transistor 200 and the third voltage-type transistor 300 are formed in the memory region 4000, the first transistor region 1000, the second transistor region 2000 and the third transistor region 3000. According to this embodiment, a semiconductor device having a memory transistor with a split-gate structure and transistors that operate at at least three different voltage levels mounted therein can be manufactured with fewer manufacturing steps.

In accordance with the manufacturing method embodiment described above, the second insulation layer 22b that forms the gate insulation layer 22 of the second voltage-type transistor 200 is formed in the same step in which the gate insulation layer 20 of the first voltage-type transistor 100 is formed. Similarly, the third insulation layer 24c that forms the gate insulation layer 24 of the third voltage-type transistor 300 and the third insulation layer 50c that forms the intermediate insulation layer 50 of the memory transistor 400 are formed in the same step in which the gate insulation layer 20 of the first voltage-type transistor 100 is formed. Also, the first through the third insulation layers 24a, 24b and 24c that form the gate insulation layer 24 of the third voltage-type transistor 300 are formed in the same steps in which the first through the third insulation layers 50a, 50b and 50c that form the intermediate insulation layer 50 of the memory transistor 400 are formed, respectively. In this manner, the gate insulation layer and the intermediate insulation layer

are formed by common steps. As a result, gate insulation layers having different dielectric strengths, in other words, different film thickness, can be formed by fewer steps.

In steps (E) and (F) in the manufacturing method embodiment described above, the silicon oxide layers 50aL and 50bL that form the first and the second insulation layers 50a and 50b of the intermediate insulation layer (tunnel insulation layer) 50 are formed, and then the second silicon nitride layer 62L is formed. As a result, the silicon oxide layers 50aL and 50bL are covered and protected by the silicon nitride layer 62L in a thermal oxidation that is later conducted or in cleaning steps before or after the thermal oxidation. Any adverse effects of the thermal oxidation step and the cleaning steps on the silicon oxide layers can be inhibited. As a result, a tunnel insulation layer having excellent characteristics can be obtained, and highly reliable memory characteristics can be realized.

Further, while the second silicon nitride layer 62L is formed on the silicon oxide layers 50aL and 50bL, a thermal treatment (including a thermal treatment in an oxidation process) is preferably conducted. As a result, the silicon oxide layers are densified and the film quality of the silicon oxide layers is improved. Thus, the memory characteristics can be improved. In particular, the number of data writing/erasing operations (cycle life) can be extended.

What is claimed:

1. A semiconductor device comprising a memory region, first, second and third transistor regions including field effect transistors that operate at different voltage levels,

the memory region including a split-gate non-volatile memory transistor,

the first transistor region including a first voltage-type transistor that operates at a first voltage level,

the second transistor region including a second voltage-type transistor that operates at a second voltage level, and

the third transistor region including a third voltage-type transistor that operates at a third voltage level,

wherein the second voltage-type transistor includes a gate insulation layer formed from at least two insulation layers, and includes gate insulation layer that is formed in the same step in which a gate insulation layer of the first voltage-type transistor is formed.

2. A semiconductor device according to claim 1, wherein the third voltage-type transistor has a gate insulation layer formed from at least three insulation layers, and includes an insulation layer that is formed in the same step in which the gate insulation layer of the first voltage-type transistor is formed.

3. A semiconductor device according to claim 2, wherein the non-volatile memory transistor comprises a source, a drain, a gate insulation layer, a floating gate, an intermediate insulation layer adapted to function as a tunnel insulation layer, and a control gate, wherein

the intermediate insulation layer is formed from at least three insulation layers, wherein first and second outermost layers of the three insulation layers respectively contact the floating gate and the control gate and are composed of insulation layers that are formed by a thermal oxidation method.

4. A semiconductor device according to claim 3, wherein the second outermost layer that contacts the control gate is formed in the same step in which the gate insulation layer of the first voltage-type transistor is formed.

5. A semiconductor device according to claim 3 , wherein the intermediate insulation layer includes an insulation layer between the first and the second outermost layers, that is formed by a CVD method.

6. A semiconductor device according to claim 5, the third voltage-type transistor has a gate insulation layer formed in the same step in which the intermediate insulation layer of the non-volatile memory transistor is formed, the gate insulation layer of the third voltage-type transistor being formed from at least three insulation layers.

7. A semiconductor device according to claim 6, wherein the first voltage-type transistor has a gate insulation layer having a thickness of 3 – 13 nm.

8. A semiconductor device according to claim 7, wherein the second voltage-type transistor has a gate insulation layer having a thickness of 4 – 15 nm.

9. A semiconductor device according to claim 8, wherein the third voltage-type transistor has a gate insulation layer having a thickness of 16 – 45 nm.

10. A semiconductor device according to claim 9, wherein the non-volatile memory transistor has an intermediate insulation layer having a thickness of 16 – 45 nm.

11. A semiconductor device according to claim 3, wherein the first outermost layer has a thickness of 5 – 15 nm, and the second outermost layer has a thickness of 1 – 10 nm.

12. A semiconductor device according to claim 1, wherein

the first voltage level that operates the first voltage-type transistor is 1.8 – 3.3 V,

the second voltage level that operates the second voltage-type transistor is 2.5 – 5 V, and

the third voltage level that operates the third voltage-type transistor is 10 – 15 V.

13. A semiconductor device according to claim 12, further comprising at least one flash-memory.

14. A semiconductor device according to claim 13, further comprising another circuit region mounted together.

15. A semiconductor device according to claim 14, wherein the another circuit region includes at least a logic circuit.

16. A semiconductor device according to claim 15, wherein the first voltage-type transistor is included in at least one circuit selected from a group consisting of a Y-gate sense amplifier, an input/output buffer, an X-address decoder, a Y-address decoder, an address buffer and a control circuit.

17. A semiconductor device according to claim 15, wherein the second voltage-type transistor is included in at least one circuit selected from a group consisting of a Y-gate sense amplifier, an input/output buffer, an X-address decoder, a Y-address decoder and an interface circuit.

18. A semiconductor device according to claim 15, wherein the third voltage-type transistor is included in at least one circuit selected from a group consisting of a voltage generation circuit, an erase voltage generation circuit and a step-up voltage circuit.

19. A semiconductor device comprising:

a memory region including a split-gate non-volatile memory transistor;

a first transistor region including a first voltage-type transistor that operates at a first voltage level;

a second transistor region including a second voltage-type transistor that operates at a second voltage level that is different than the first voltage level; and

a third transistor region including a third voltage-type transistor that operates at a third voltage level that is different than the second voltage level;

wherein the second voltage-type transistor includes a gate insulation layer formed from at least two insulation layers.

20. A semiconductor device according to claim 19, wherein the third voltage-type transistor has a gate insulation layer formed from at least three insulation layers.

21. A semiconductor device according to claim 19, wherein the non-volatile memory transistor comprises a source, a drain, a gate insulation layer, a floating gate, an intermediate insulation layer adapted to function as a tunnel insulation layer, and a control gate, wherein

the intermediate insulation layer is formed from at least three insulation layers, wherein a first insulation layer contacts the floating gate and a third insulation layer contacts the control gate.

22. A semiconductor device as in claim 19, wherein the first voltage level is in the range of 1.8 to 3.3 V, the second voltage level is in the range of 2.5 to 5 V, and the third voltage level is in the range of 10 to 15 V.

23. A embedded semiconductor device comprising:

a plurality of semiconductor devices selected from the group consisting of a flash-memory, an SRAM memory, a RISC, an analog circuit, and an interface circuit;

the plurality of semiconductor devices being embedded in a sea of gates structure;

wherein at least one of the semiconductor devices comprises the structure of claim 19.

Abstract

Embodiments include a semiconductor device having a non-volatile memory transistor, the semiconductor device including a plurality of field effect transistors operated at a plurality of different voltage levels. The semiconductor device has a memory region 4000, and first, second and third transistor regions 1000, 2000 and 3000 respectively including field effect transistors that operate at different voltage levels. The memory region 4000 includes a split-gate non-volatile memory transistor 400. The first transistor region 1000 includes a first voltage-type transistor 100 that operates at a first voltage level. The second transistor region 2000 includes a second voltage-type transistor 200 that operates at a second voltage level. The third transistor region 3000 includes a third voltage-type transistor that operates at a third voltage level. The second voltage-type transistor 200 has a gate insulation layer 22 that is formed from at least two insulation layers 22a and 22b. The insulation layer 22b is formed in the same step in which a gate insulation layer 20 of the first voltage-type transistor 100 is formed.

Fig. 1

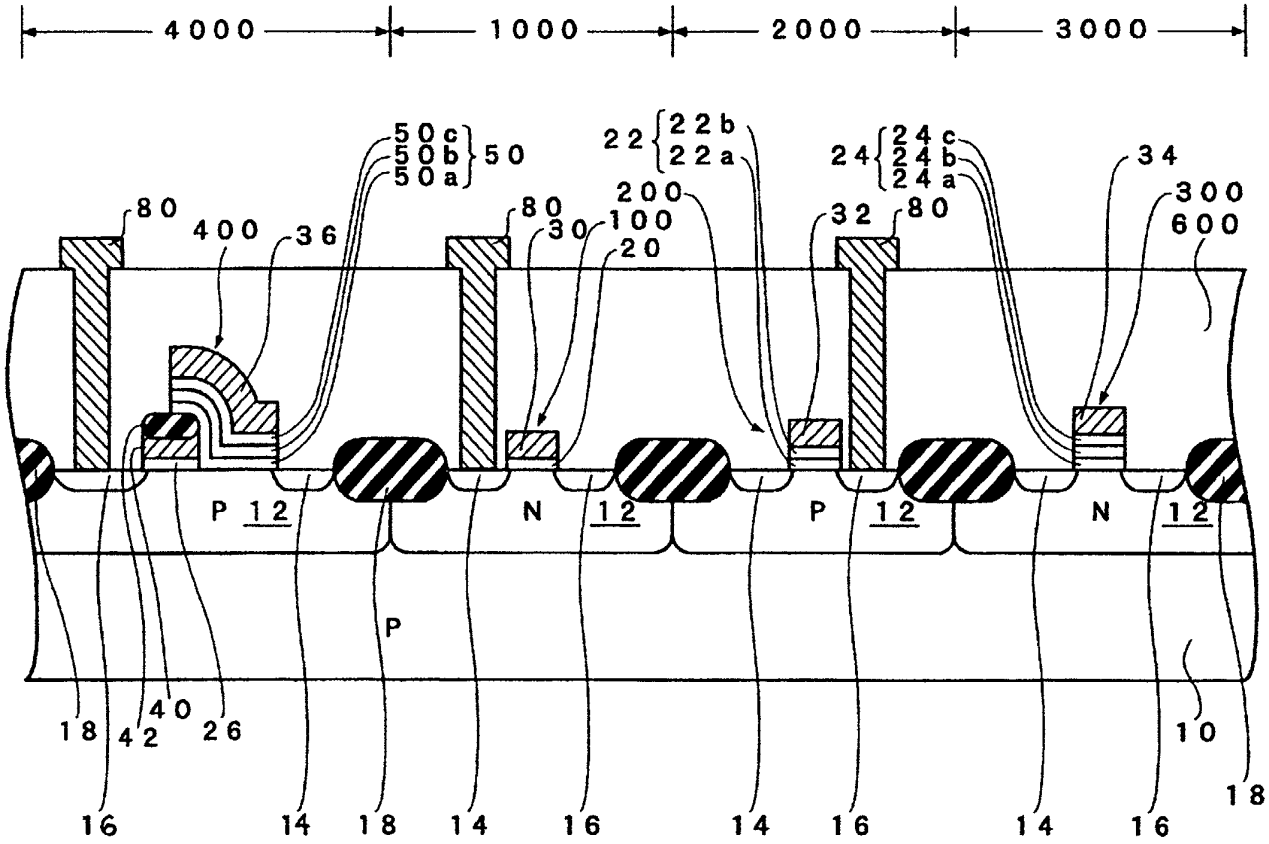

4000
1000
2000
3000
50c
50b
50a
50
22
22b
22a
24
24c
24b
24a
34
300
600
80
400
36
80
30
100
20
200
32
80
P 12
N 12
P 12
N 12
P
18
42
40
26
10
16
14
18
14
16
14
16
14
16
18

Fig. 2

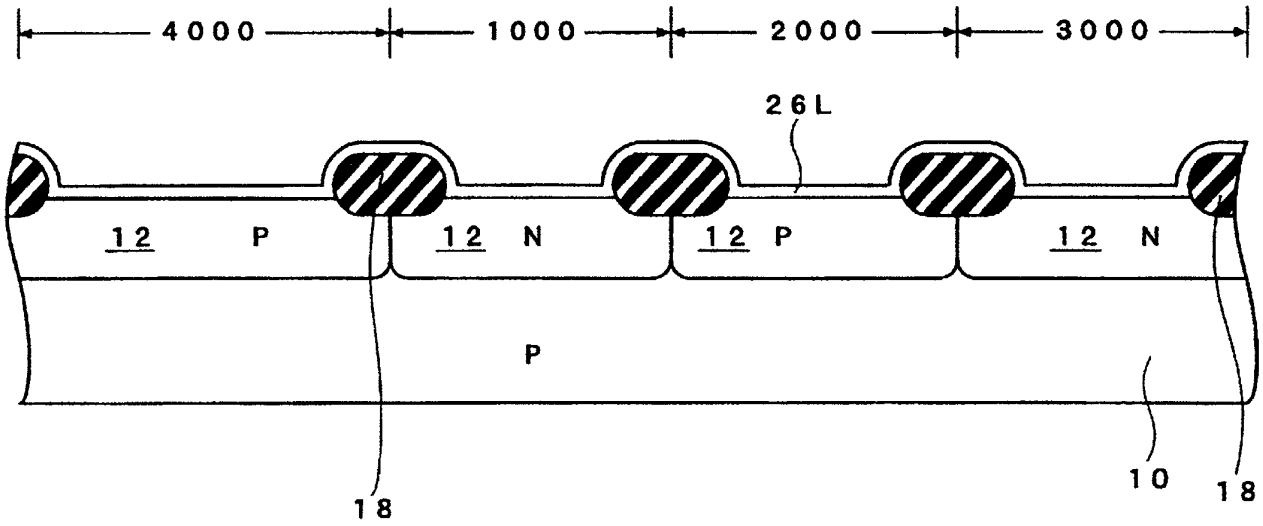


Fig. 3

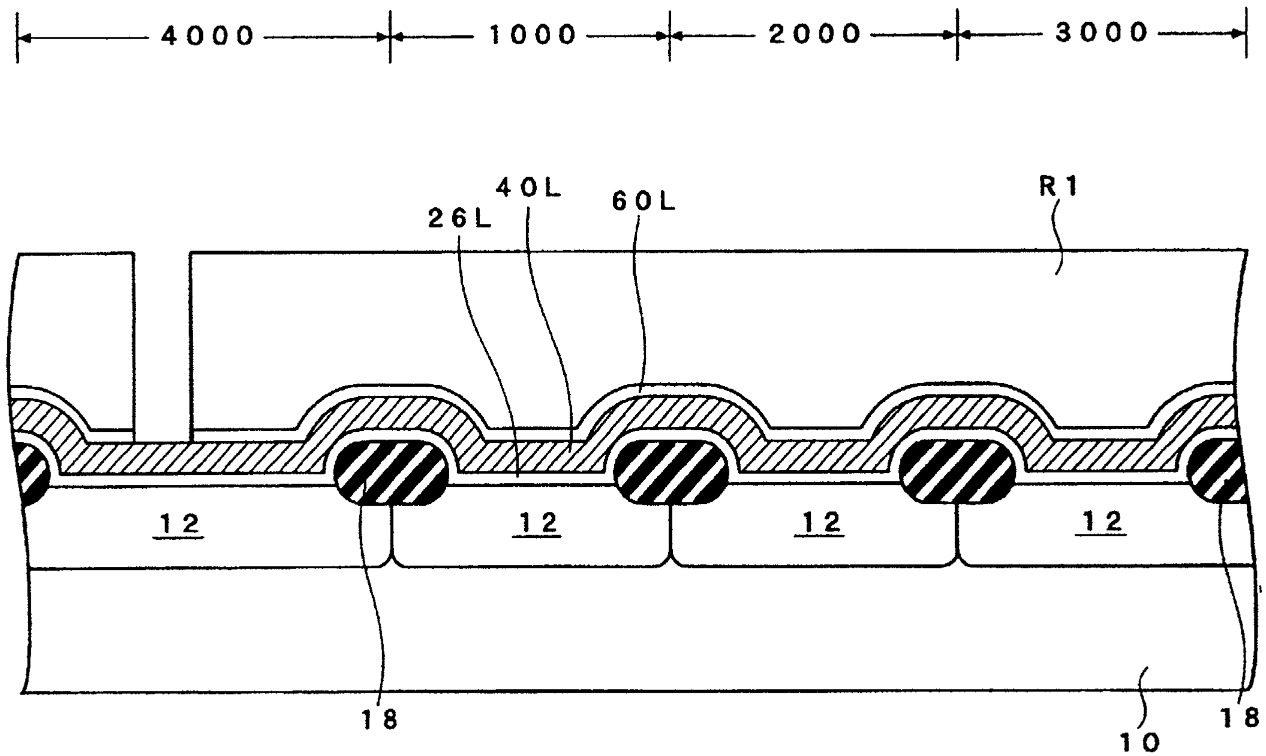


Fig. 4

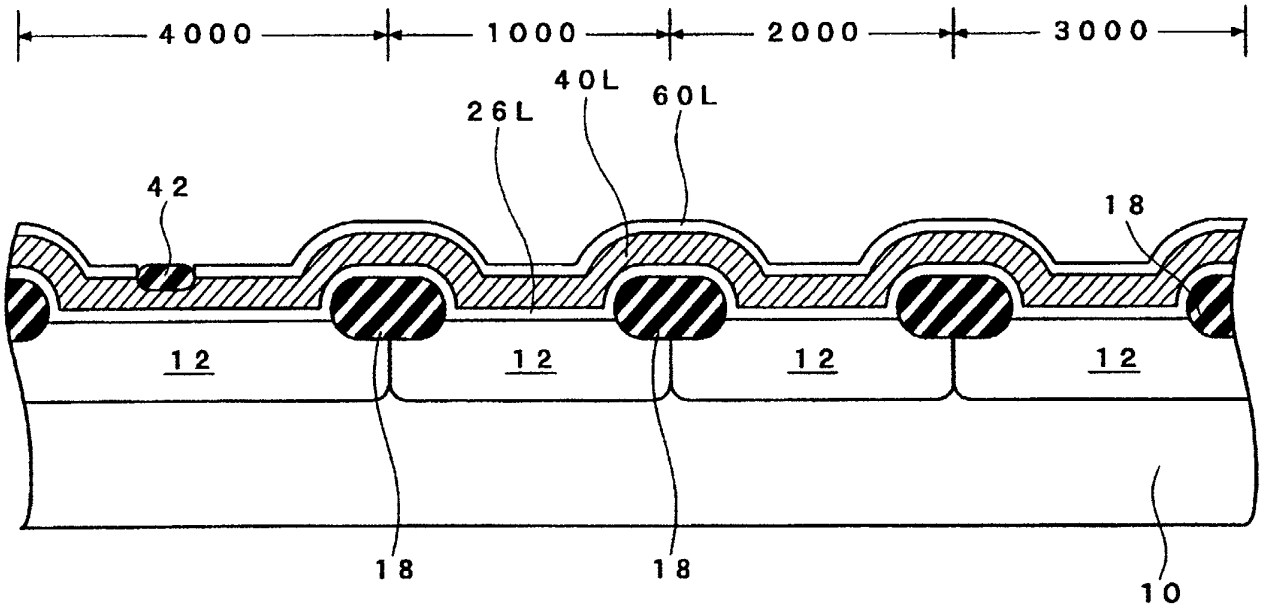


Fig. 5

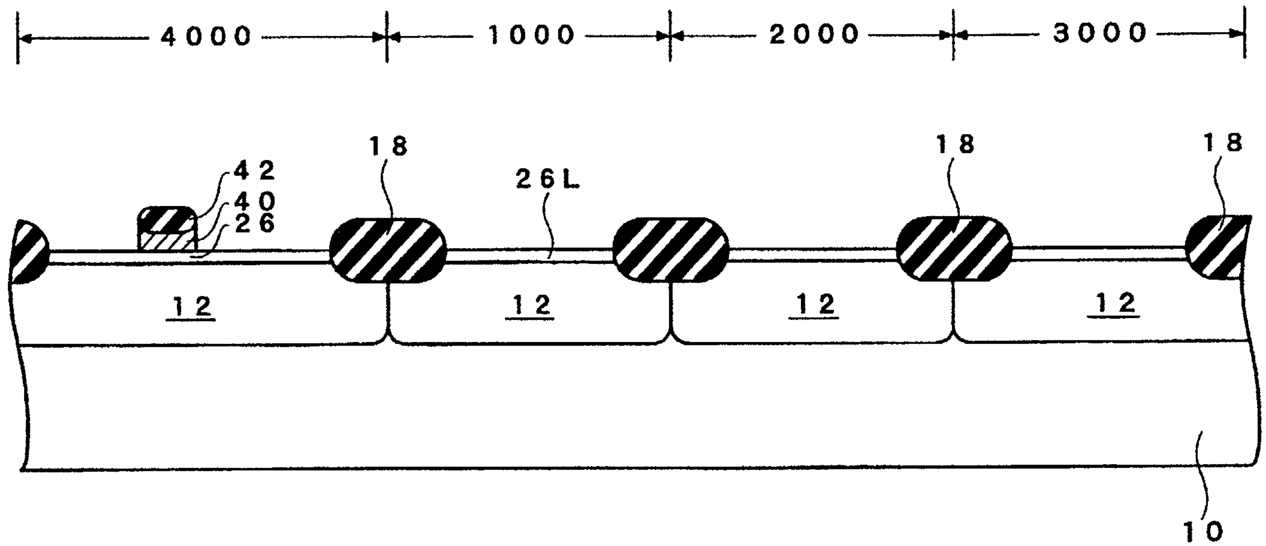


Fig. 6

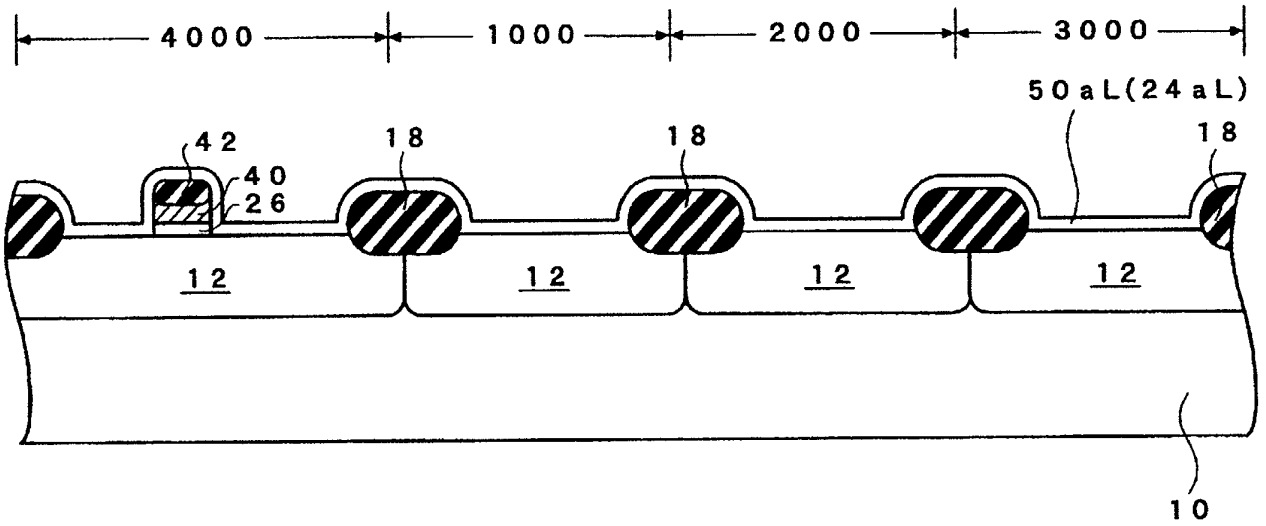


Fig. 7

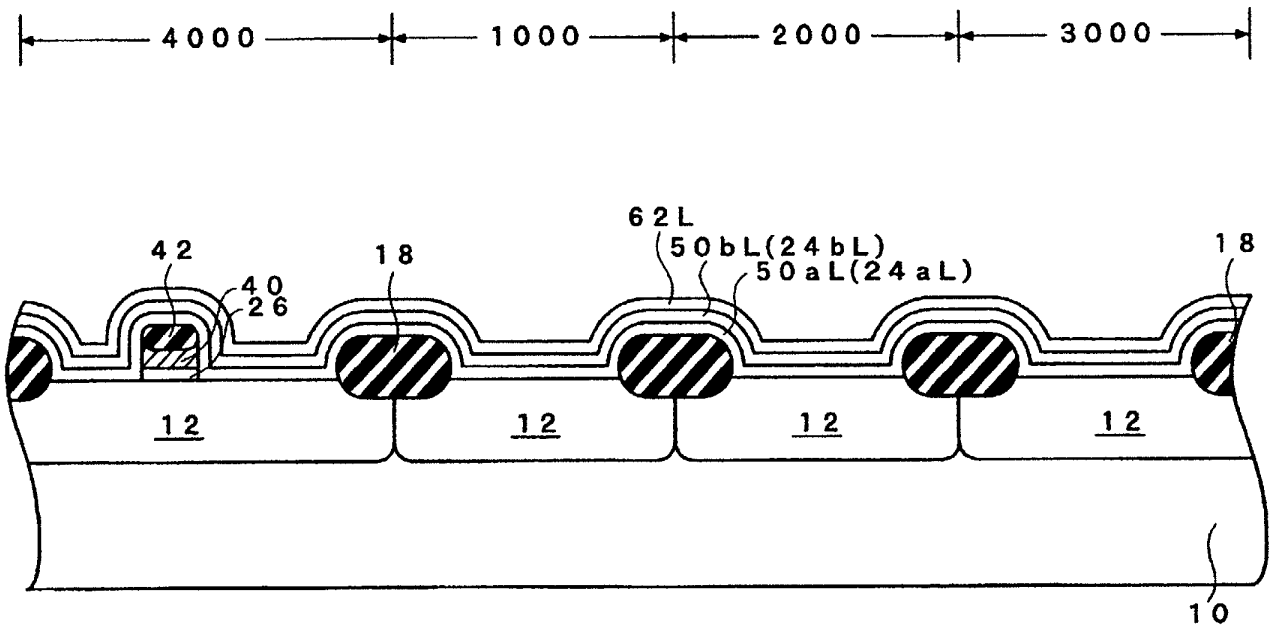

4000
1000
2000
3000
42
40
26
18
62L
50bL(24bL)
50aL(24aL)
18
12
12
12
12
10

Fig. 8

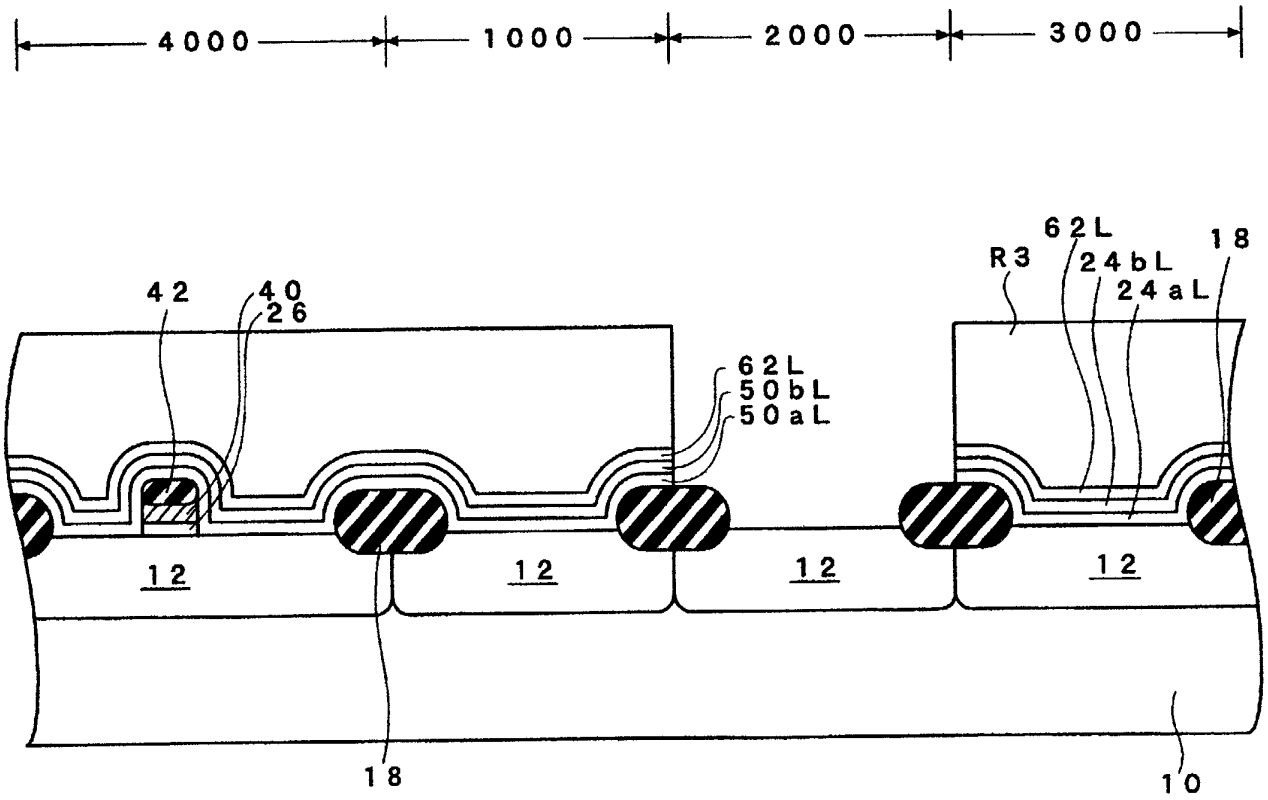

4000
1000
2000
3000
42
40
26
62L
50bL
50aL
R3
62L
24bL
24aL
18
12
12
12
12
18
10

Fig. 9

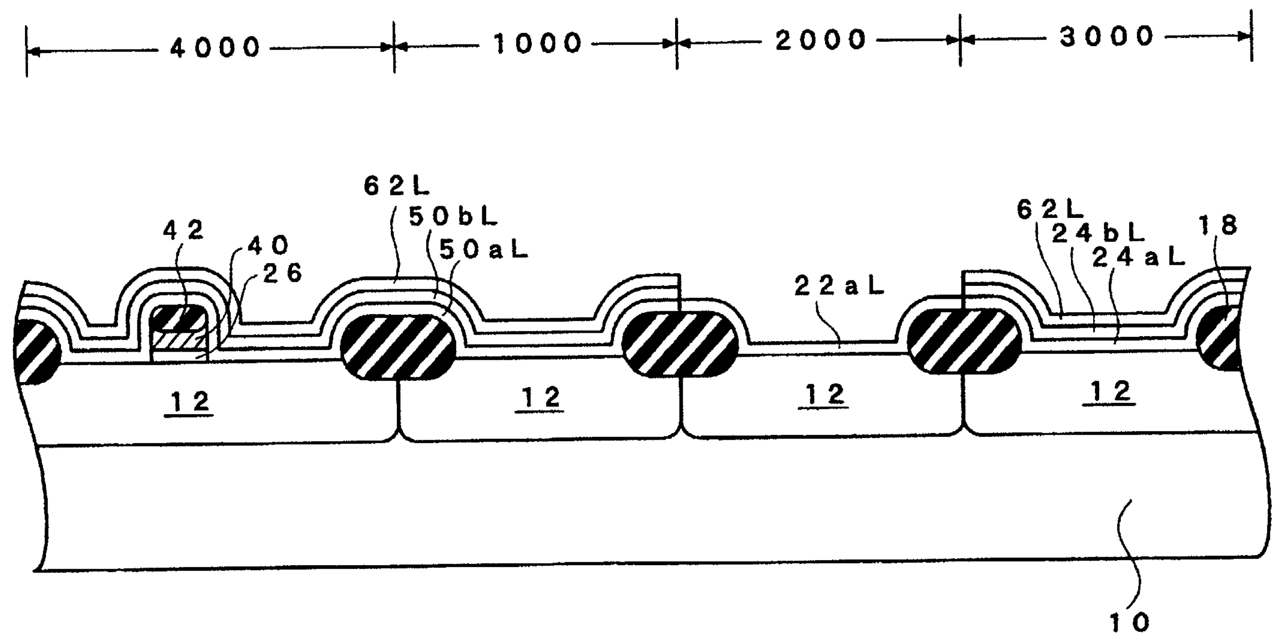

4000
1000
2000
3000
62L
50bL
50aL
42
40
26
22aL
62L
24bL
24aL
18
12
12
12
12
10

Fig. 10

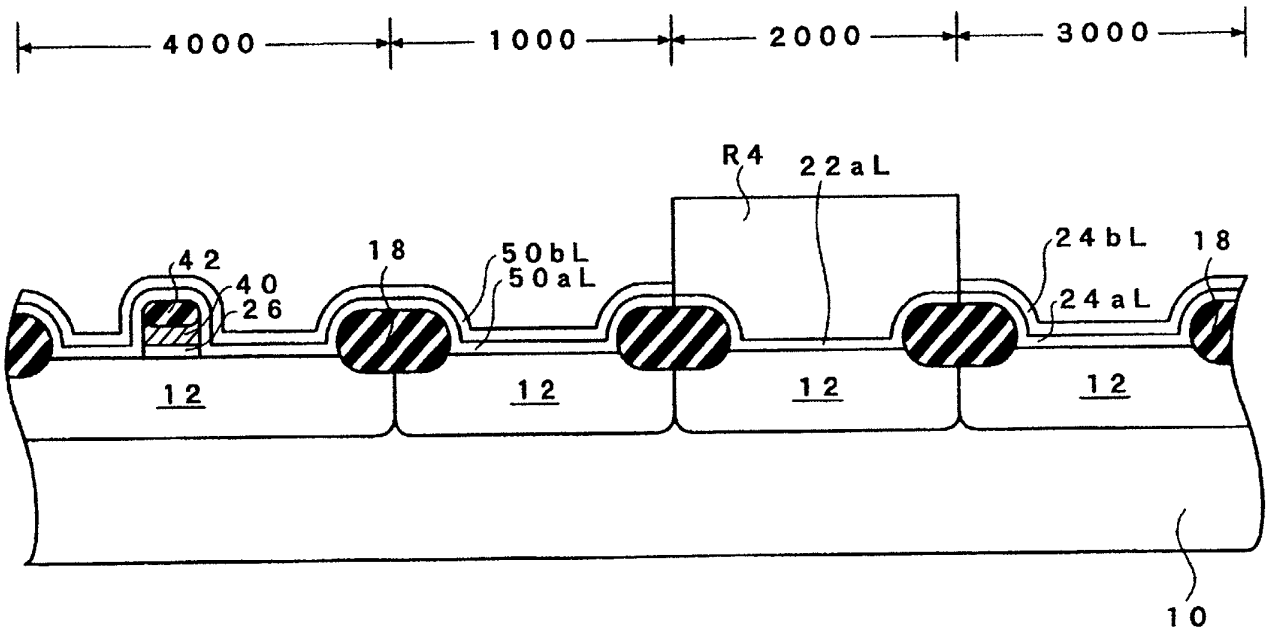

4000
1000
2000
3000
R4
22aL
42
40
26
18
50bL
50aL
24bL
24aL
18
12
12
12
12
10

Fig. 11

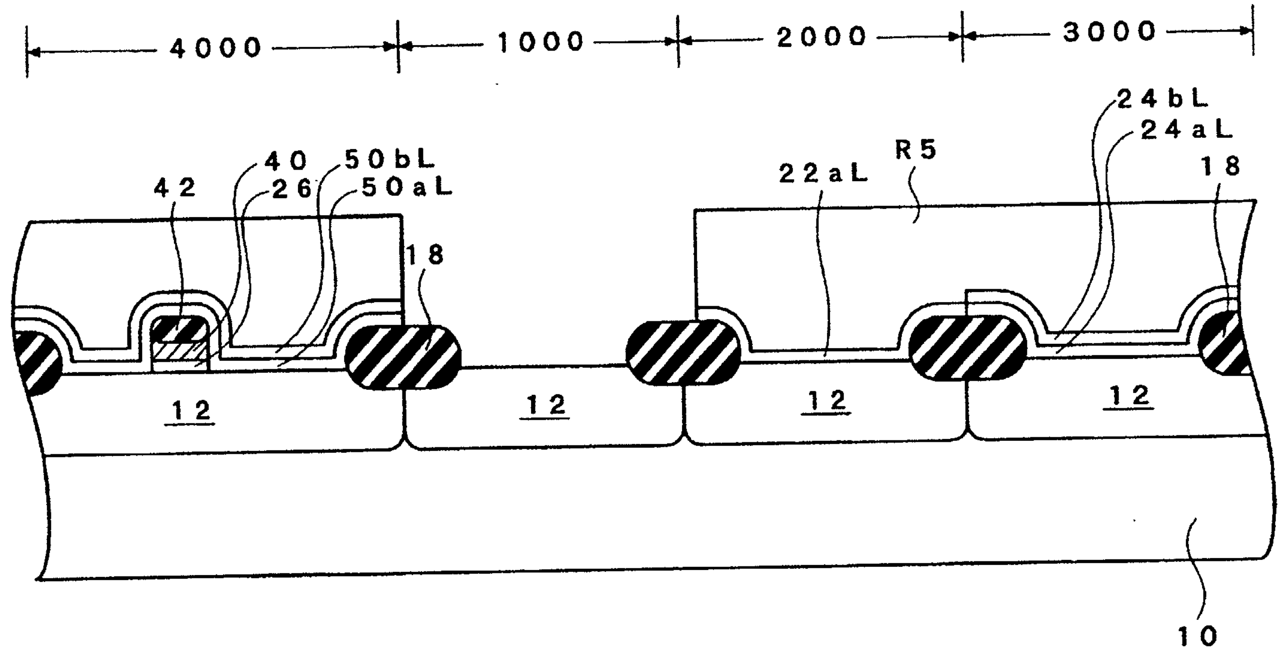

4000
1000
2000
3000
42
40
26
50bL
50aL
18
22aL
R5
24bL
24aL
18
12
12
12
12
10

Fig. 12

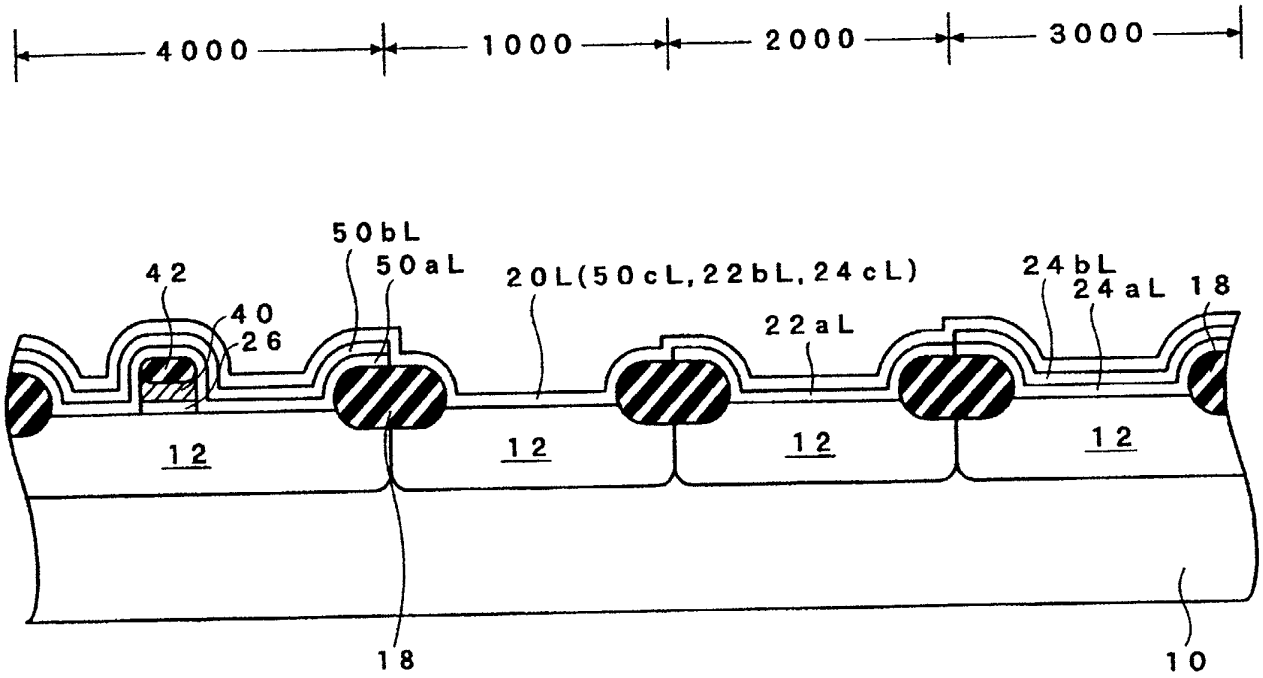
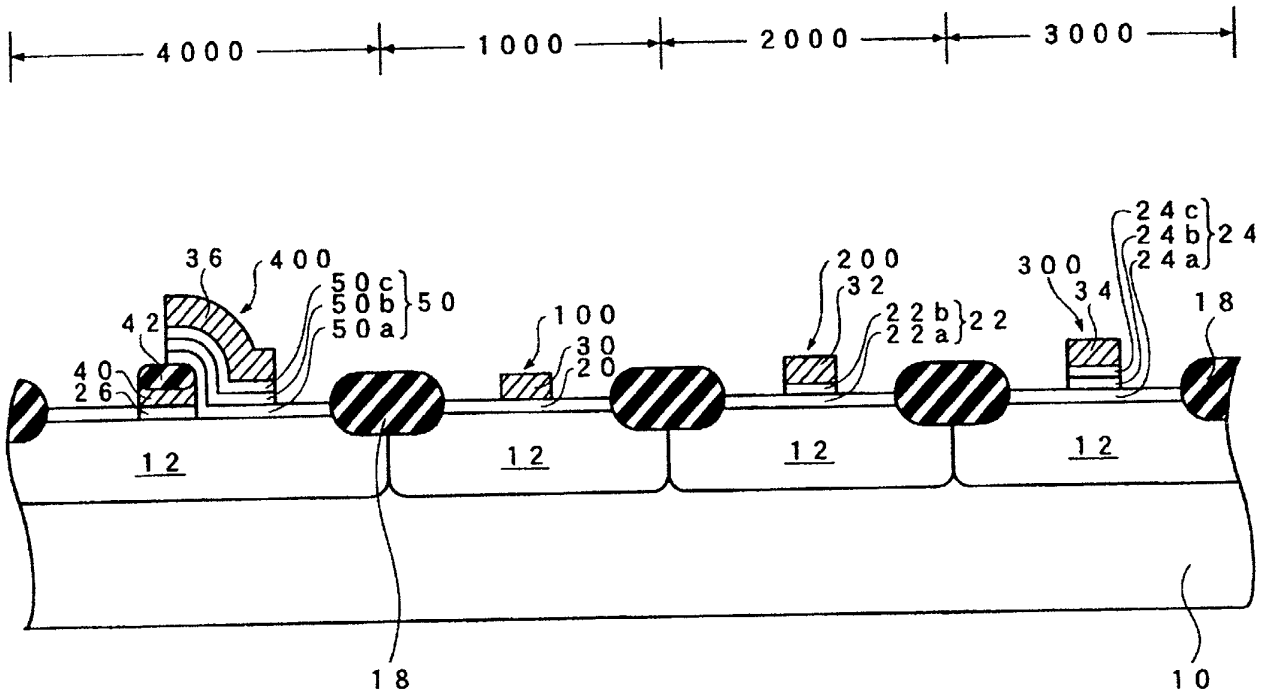

4000
1000
2000
3000
50bL
50aL
42
40
26
20L(50cL, 22bL, 24cL)
22aL
24bL
24aL
18
12
12
12
12
18
10

Fig. 13


4000
1000
2000
3000
36
400
50c
50b
50a
50
42
40
26
100
30
20
200
32
22b
22a
22
300
34
24c
24b
24a
24
18
12
12
12
12
18
10

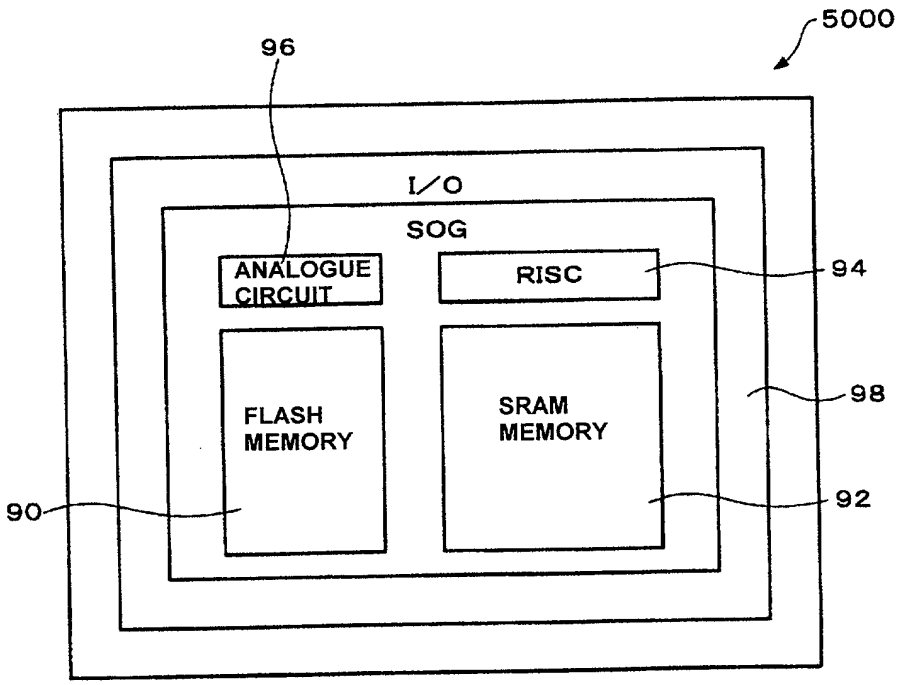

5000
96
I/O
SOG
ANALOGUE CIRCUIT
RISC
94
FLASH MEMORY
SRAM MEMORY
98
90
92

Fig. 14

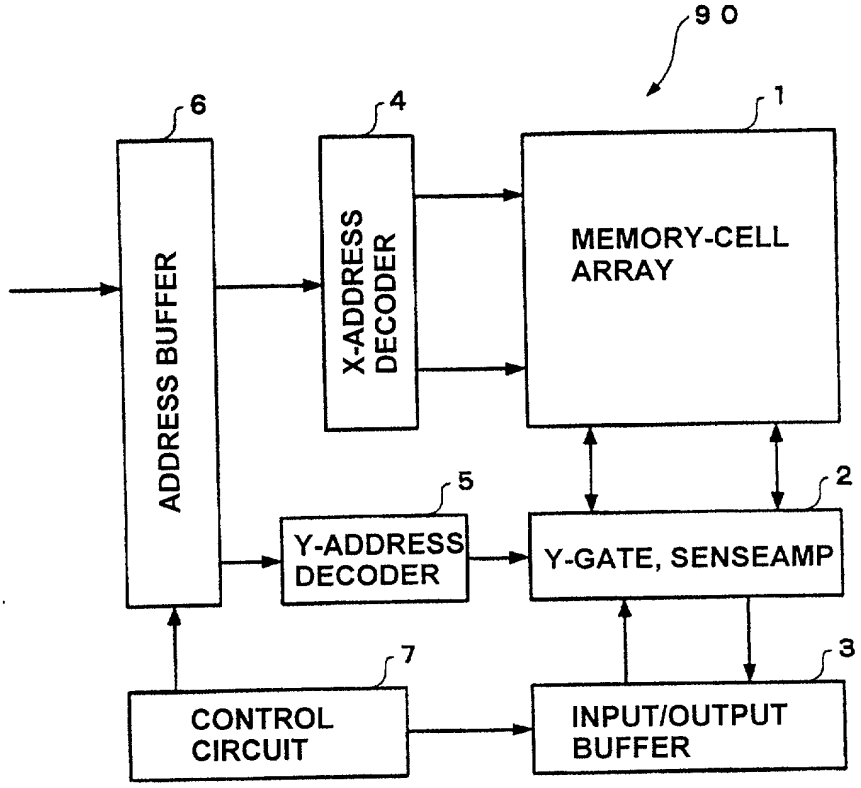

90
6
4
1
ADDRESS BUFFER
X-ADDRESS DECODER
MEMORY-CELL ARRAY
5
2
Y-ADDRESS DECODER
Y-GATE, SENSEAMP
7
3
CONTROL CIRCUIT
INPUT/OUTPUT BUFFER

FIG. 15